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Design and Simulation of High Gain Two Stage CMOS Operational Amplifier in 130nm CMOS

K. Lokesh Krishna[1], **D.** Srihari[2], P. Lavanya[3]

[1]*Department of ECE S.V.C.E.T.(Autonomous), Chittoor, Andhra Pradesh*
[2]*Department of ECE S.E.A.G.I., Tirupati Andhra Pradesh*
[3]*M.Tech Student, VLSI Design Department of ECE S.V.C.E.T.(Autonomous), Chittoor, Andhra Pradesh*
E-mail: [1]kayamlokesh78@gmail.com, [3]plavanyareddy426@gmail.com

Abstract: *This paper presents the design and simulation of a high gain and low power two stage operational amplifier in 180nm CMOS technology. High gain enables the circuit to operate efficiently in a closed loop feedback system. The designed operational amplifier is modeled using Cadence Virtuoso schematic editor and simulated using Cadence Spectre, while the layout has been developed using Virtuoso. A RC Miller compensation technique is adopted by connecting a compensating capacitor across high gain stage to optimize variations in gain and bandwidth for high speed applications. The designed op-amp provides a DC gain of 65dB and a unity gain bandwidth of 100MHz at 2pF. The power consumption is found to be 16.46µW, slew rate is 26V/µs and area occupied is 12µm×16µm.*

1. INTRODUCTION

High gain and low power Operational Amplifiers (Op-Amps) are very much essential to various mixed signal systems. They play a vital role in the amplification of the signal. Op-amps are used in many applications such as high speed Analog to Digital converters, Digital to Analog converters, filters, linear applications such as summers, integrators, differentiators, comparators, buffers, negative impedance converters and non-linear applications such as clippers, clampers, multivibrators, log amplifiers, antilog amplifiers and electronic analog computation. These circuits are implemented using a variety of architectures, sizes and speeds. So the design of op-amps with low power, high gain and high bandwidth are very much critical in many mixed mode signal applications. With the rapid improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, miniaturization in transistor scaling, and the developments in fabrication processes, the integrated circuit market is growing rapidly. Nowadays, Complementary Metal-Oxide Semiconductor (CMOS) technology has become dominant over Bipolar (BJT) technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to design. Scaling down of CMOS feature sizes results in higher unity gain frequency (f_T) which means the transistors operate faster than before. However, this is achieved at the cost of a reduction in transistor's open loop gain (A_{OL}) [1]. Also due to scaling power supply voltage can be reduced. So because of this the battery size and weight reduces and enables longer battery life time. Hence for the same reason, low-powered circuits reduce thermal dissipation. Thus amplifiers designed in smaller device lengths exhibit larger bandwidths but lower open loop gain [2]. Finally in most of the mixed signal systems, the design of high gain, low power and wide bandwidth op-amps are crucial.

This paper is organized as follows. Section II discusses the block diagram of two stage CMOS operational amplifier. Section III presents the obtained simulation results of the designed op-amp. Also section III contains the various performance results of designed op-amp. Finally, conclusions are drawn in Section IV.

2. TWO STAGE CMOS OP-AMP.

An operational amplifier is a high gain DC coupled electronic voltage amplifier with a differential input and, usually, a single-ended output. Basically, Op Amps are voltage amplifiers being used for achieving high gain by applying differential inputs. The gain is typically between 60 to 80 decibels. This means that even very small voltage difference between the input terminals drives the output voltage to the supply voltage. To achieve a higher gain, multi-stage op-amp can be used by cascading the stages where voltage gain can reach upto 120 dB [3-4]. If gain increases, then bandwidth decreases. However, it becomes very difficult to compensate and stabilize a two stage op-amp, which is widely used in many applications. Furthermore, since op-amps are designed to operate with negative-feedback connection, frequency compensation is very much essential for closed-loop stability [5-7]. In designing an op-amp, various electrical characteristics such as slew rate, common mode range, output

swing, gain bandwidth product, offset voltages and currents etc., all have to be taken into consideration [8-11].In this paper, a fully differential compensated two-stage CMOS op-amp is designed and simulated. The fully differential topology exhibits high gain, high bandwidth and occupies less area.

2.1 Various Op-Amp topologies:

There are a wide range of op-amp topologies. Table 1 shows the comparison between performances of different op-amp topologies.

Table 1: Comparison between performances of different op-amp topologies.

Type of op-amp	Gain	Output swing	Speed	Power consumption	Noise
Folded Cascode	Medium	Medium	High	Medium	Medium
Telescopic	Medium	Low	Highest	Low	Low
Gain Boosted	High	Medium	Medium	High	Medium
Two-Stage	High	Highest	Low	Medium	Low

From the table 1, telescopic op-amp offers the best design, but the telescopic designed op-amp suffers from low output voltage swing and medium gain despite its low power, high speed and low noise. So a two stage op-amp topology offers the best design, as it has high gain, highest output voltage swing, low noise and reduced power consumption. In this paper, a fully differential compensated two-stage CMOS op-amp is designed and simulated. The fully differential topology exhibits high gain, high bandwidth, reduced power consumption and occupies less area.

The simplified block diagram of general two stage op-amp is shown in Fig. 1.

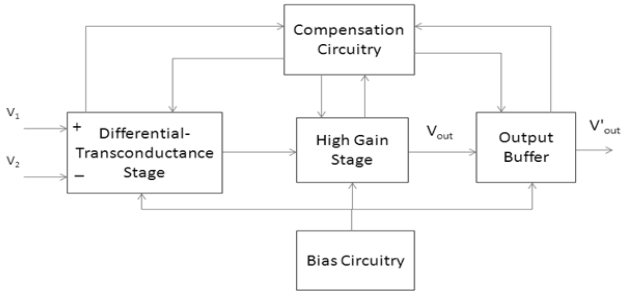

Fig. 1: Block diagram of general two stage op-amp

The first block is a differential transconductance amplifier. It has two inputs which are the inverting input voltage (V_1) and non-inverting input voltage (V_2). It provides at the output a differential voltage or a differential current that, essentially, depends on the differential input only. The next block is a differential to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended version. In most cases if the gain provided by the input stages is not sufficient, then additional amplification is provided by intermediate stage, which is another differential amplifier, driven by the output of the first stage.

The purpose of biasing circuitry is to establish the proper operating point for each transistor in its saturation region. Finally, we have the output buffer stage. It provides the low output impedance and larger output current needed to drive the load of op-amp or improves the slew rate of the op- amp. The purpose of the compensation circuitry is to lower the gain at high frequencies and to maintain stability when negative feedback is applied to the op-amp.

The Schematic diagram of general unbuffered two stage CMOS operational amplifier is shown in Fig. 2 [9]. It consists of three sub sections namely differential gain stage, second gain stage and bias circuitry.

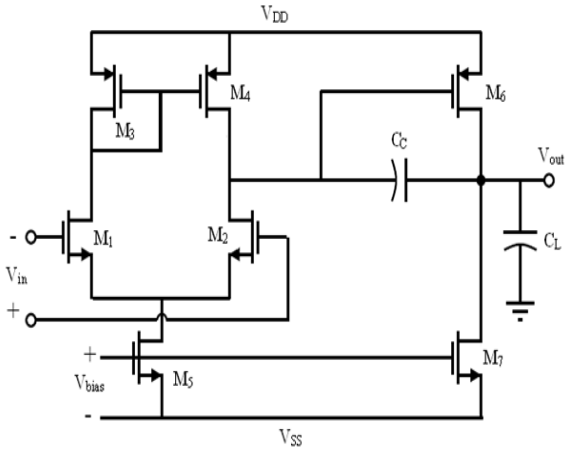

Fig. 2: Unbuffered, two stage CMOS op-amp

2.2 Differential Gain Stage

Transistors M_1, M_2, M_3 and M_4 form the first stage of the op amp of the differential amplifier with differential to single ended transformation. Transistors M_1 and M_2 are standard N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. M_3 and M_4 form a current mirror that acts as the active load for M_1 and M_2. The gate of M_1 is the inverting input and the gate of M_2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of the stage is simply the transconductance of M_2 times the total output resistance seen at the drain of M_2. The two main resistances that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the active load transistors, M_3 and M_4. The current from M_1 is mirrored by M_3 and M_4 and subtracted from the current from M_2. The differential current from M_1 and M_2 multiplied by the output

resistance of the first stage gives the single-ended output voltage, which constitutes the input to the second gain stage.

2.3 Second Gain Stage

The second stage is a current sink load inverter. The main purpose of the second gain stage, as the name it implies, is to provide additional gain in the amplifier. It consists of transistors M_6 and M_7. This stage takes the output from the drain of M_2 and amplifies it through M_6 which is in the standard common source configuration. M_6 is the common source gain stage and it is also the second gain stage. Again, similar to the differential gain stage, this stage employs an active device M_7, to serve as the load resistance for M_6. M_6 is the driver while M_7 acts as the load. The gain of this second stage is transconductance of M_6 times the equivalent load resistance seen at the output side of M_6 and M_7.

2.4 Bias Circuitry

The biasing of the operational amplifier is done with one or two additional transistors in the section V_{bias}. Transistors M_6 and M_7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string.

3. SIMULATION RESULTS AND DISCUSSIONS:

The schematic diagram of two stage CMOS op-amp shown in Fig. 3 is modeled using Virtuoso schematic editor and simulated using Cadence Spectre, while the layout has been developed using Virtuoso. The circuit is operated from a 1.5V power supply. The achieved parameters from the operational amplifier simulation are given in Table 1.

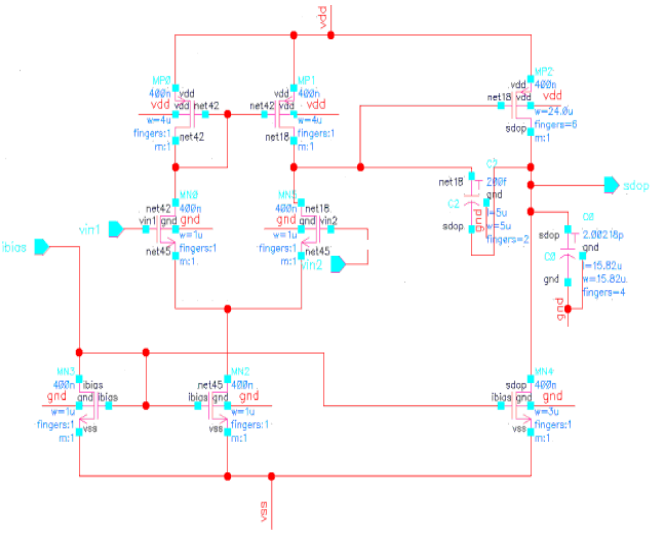

Fig. 3: Schematic diagram of two stage operational amplifier circuit

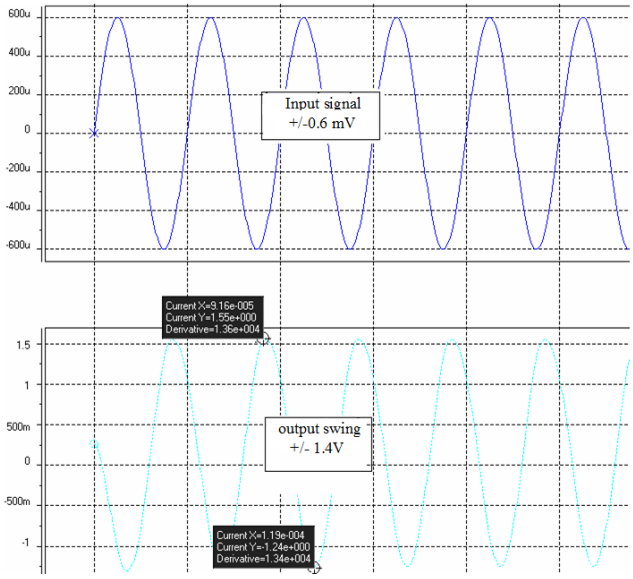

Fig. 4: Transient analysis

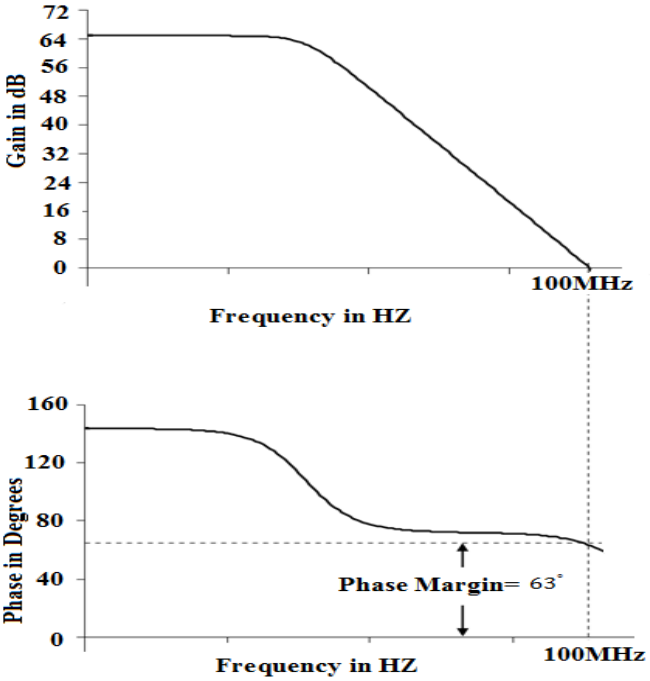

Fig. 5: Simulated magnitude and phase response

Fig. 4 shows the simulated transient analysis of op-amp and Fig. 5 shows the simulated magnitude and phase response of the designed op-amp. From the response unity gain bandwidth and phase margin has been found to be 1MHz and 63°. The pre layout and post layout simulation results show that the designed op-amp achieves a higher gain and a larger bandwidth. Table 2 presents the various obtained parameters of the designed op-amp.

Table 2: Achieved values from simulation

Parameter	Simulated results
Technology	0.13µm CMOS
Gain	65dB
Slew rate	26v/µs
Unity Gain bandwidth	100MHz
CMRR	68dB
Phase Margin	63°
Input swing	+/-0.6mV
Output swing	+/-1.4V
Power dissipation	16.46µW
Area	12µm ×16µm

4. CONCLUSION

In this paper a high gain, high speed and low power two stage operational amplifier in 130nm CMOS is designed and simulated. Simulation results confirm that the designed op-amp achieves high gain, high slew rate, low power, better CMRR and occupies less area. By redesigning the bias currents of the transistors, the circuit can be made to operate at higher bandwidth. The gain of the op-amp can be increased further by cascading another device in the input stage. Also the output voltage swing may be increased by using a double ended output.

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